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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SONG, JASMINE	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,376	PURCELL ET AL.	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *21-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This office action is in response to RCE filed 08/18/2005, claims 21-24 have been canceled, therefore, claims 1-20 and 25 are pending in the application. All rejections and objections not explicitly repeated below are withdrawn.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-6,13-18 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Novak et al., U.S. Patent 6,295,586 B1.

Regarding claim 1, Novak teaches that an apparatus comprising:

a queue (one of the AQ 340, PQ 350 and RWQ 360 as shown in the Fig.2) storing a plurality of memory transactions (col.9, lines 3) to be sent over a memory bus (Fig.1 or Fig.2, element 100) to a memory having a plurality of memory banks(Fig.1, element 70, col.6, lines 32-34), each memory transaction addressed to one of the memory banks (col.6, lines 53-56 and lines 63-64 and col.7, lines 9-11 and lines 46-53); and

an arbiter (Fig.2, SPM 370) simultaneously coupled to each of the plurality of memory transactions (it is inherent that the SPM 370 coupled to each of the plurality of memory transaction since the SPM 370 selects an operation to be sent to the memory, in order to select an operation, SPM has to coupled to each memory transactions simultaneously) and configured to generate a plurality of bank readiness signals (it is taught as the requester send to the arbiter will assert the bank readiness signals), each bank readiness signal indicating the readiness of one of the memory banks to accept a memory transaction (col.11, lines 14-17), and

select one of the memory transactions for transmission over the memory bus based on the bank readiness signals (col.11, lines 17-22).

Regarding claim 2, Novak teaches that further comprising:

a memory controller (Fig.1, element 200, col.5, lines 23-30) configured to send the selected memory transaction (the selected operation with highest priority) over the memory bus (Fig.1 or Fig.2, element 100).

Regarding claim 3, Novak teaches that further comprising:

a queue controller (Fig.2, element 365) configured to associate with each of the memory transactions a different priority in a set of priorities (col.9, lines 11-19); and wherein

the arbiter (Fig.2, element 370) is further configured to select the one of the memory transactions when the bank readiness signal indicates that the memory bank to which the one of the memory transactions is destined is ready to accept a memory transaction and the priority associated with the one of the memory transactions is greater than a priority associated with any of the other memory transactions (col.11, lines 12-22).

Regarding claim 4, Novak teaches that wherein:

each priority represents an age of a memory transaction is taught as each entries in the operation queue has a priority and strictly adhering to timing dependency (col.9, lines 5-19).

Regarding claim 5, Novak teaches that wherein:

The plurality of memory transactions enter the queue at a first request station and progress toward a second request station until selected for transmission over the memory bus based on the bank readiness signals (col.7, lines 46-49).

Regarding claim 6, Novak teaches that wherein:

the arbiter is further configured to send a memory transaction to a memory bank, clear the bank readiness signal for the memory bank at approximately the time of sending the memory transaction to the memory bank, and set the bank readiness signal for the memory bank a predetermined period of time after sending the memory transaction to the memory bank (col.9, lines 22-26 and col.11, lines 12-22).

Regarding claim 13, Novak teaches that a method comprising:

identifying a plurality of memory transactions (col.9, lines 3, the queued operations within three queue as shown in the Fig.2) to be sent over a memory bus (Fig.1 or Fig.2, element 100) to a memory having a plurality of memory bank (Fig.1, element 70, col.6, lines 32-34), each memory transaction addressed to one of the memory banks (col.6, lines 53-56 and lines 63-64 and col.7, lines 9-11 and lines 46-53);

generating a plurality of bank readiness signals based upon a content of the memory bus (col.7, lines 44-45 and lines 51-53, since only one bank of one CS can send or receive data over the memory bus, therefore, by monitoring the content of memory bus will know a plurality of bank access and then generating a plurality of bank readiness signals), each bank readiness signal generated using an arbiter simultaneously coupled to each of the plurality of memory transactions (it is inherent that the SPM 370 coupled to each of the plurality of memory transaction since the SPM 370 selects an operation to be sent to the memory, in order to select an operation, SPM has to coupled to each memory transactions simultaneously) and indicating the

readiness of one of the memory banks to accept a memory transaction (col.11, lines 14-17); and

selecting one of the memory transactions for transmission over the memory bus based on the bank readiness signals (col.11, lines 17-22).

Regarding claim 14, Novak teaches that further comprising:

sending the selected memory transaction (the selected operation with highest priority) over the memory bus (Fig.1 or Fig.2, element 100).

Regarding claim 15, Novak teaches that wherein each of the memory transactions is associated with a different priority in a set of priorities (col.9, lines 11-19), and wherein selecting further comprises:

selecting the one of the memory transactions when the bank readiness signal indicates that the memory bank to which the one of the memory transactions is destined is ready to accept a memory transaction and the priority associated with the one of the memory transactions is greater than a priority associated with any of the other memory transactions (col.11, lines 12-22).

Regarding claim 16, Novak teaches that further comprising:

associating the priorities with the memory transactions based on an age of the memory transactions is taught as each entries in the operation queue has a priority and strictly adhering to timing dependency (col.9, lines 5-19).

Regarding claim 17, Novak teaches that the content of the memory bus comprises an address of a memory transaction monitored by a state machine (it is implied in the reference because an address of a memory transaction has to be known in order to select one request to be sent to the SMC).

Regarding claim 18, Novak teaches that wherein generating comprises:

sending a memory transaction to a memory bank; clearing the bank readiness signal for the memory bank at approximately the time of sending the memory transaction to the memory bank; and setting the bank readiness signal for the memory bank a predetermined period of time after sending the memory transaction to the memory bank (col.9, lines 22-26 and col.11, lines 12-22).

Regarding claim 20, Novak teaches that the plurality of memory transactions are sent over the memory bus one memory transaction at a time (col.7, lines 51-53).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7-12,19 and 25 rejected under 35 U.S.C. 103(a) as being unpatentable over Novak et al., U.S. Patent 6,295,586 B1, in view of Fenwick et al., US Patent 6,076,129.

Regarding claims 7,19 and 25, Novak teaches that a method comprising:

identifying a plurality of memory transactions (col.9, lines 3, the queued operations within three queue as shown in the Fig.2) to be sent over a memory bus (Fig.1 or Fig.2, element 100) to a memory having a plurality of memory bank (Fig.1, element 70, col.6, lines 32-34), each memory transaction addressed to one of the memory banks (col.6, lines 53-56 and lines 63-64 and col.7, lines 9-11 and lines 46-53);

generating a plurality of bank readiness signals by monitoring the memory bus (col.7, lines 44-45 and lines 51-53, since only one bank of one CS can send or receive data over the memory bus, therefore, by monitoring the memory bus will know a plurality of bank access and then generating a plurality of bank readiness signals), each bank readiness signal indicating the readiness of one of the memory banks to accept a memory transaction (col.11, lines 14-17); and

selecting one of the memory transactions for transmission over the memory bus based on the bank readiness signals (col.11, lines 17-22).

Novak does not teach that generating a plurality of bank readiness signals by monitoring the addresses of the plurality of memory transactions gated across the memory bus at a location along the memory bus.

However, Fenwick teaches generating a plurality of bank readiness signals by monitoring the addresses of the plurality of memory transactions gated across the

memory bus at a location along the memory bus (col.9, lines 1-6 and lines 20-42 and col.18, lines 45-50).

It would have been obvious to one having ordinary skill at the time the invention was made to utilize the teachings of Fenwick in the system of Novak and generating a plurality of bank readiness signals by monitoring the addresses of the plurality of memory transactions gated across the memory bus at a location along the memory bus because the interdependency of the address and data portion of the typical system bus protocol can adversely affect the overall performance of the bus, with the arrangement of monitoring the addresses of the plurality of memory transactions gated across the memory bus will allowing independent operation of the address bus, thereby improve the overall performance of the bus (col.1, lines 47-49 and 53-58).

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 8, Novak teaches that further comprising:

sending the selected memory transaction (the selected operation with highest priority) over the memory bus (Fig.1 or Fig.2, element 100).

Regarding claim 9, Novak teaches that wherein each of the memory transactions is associated with a different priority in a set of priorities (col.9, lines 11-19), and wherein selecting further comprises:

selecting the one of the memory transactions when the bank readiness signal indicates that the memory bank to which the one of the memory transactions is destined is ready to accept a memory transaction and the priority associated with the one of the memory transactions is greater than a priority associated with any of the other memory transactions (col.11, lines 12-22).

Regarding claim 10, Novak teaches that further comprising:

associating the priorities with the memory transactions based on an age of the memory transactions is taught as each entries in the operation queue has a priority and strictly adhering to timing dependency (col.9, lines 5-19).

Regarding claim 11, Novak teaches that generating comprising:

generating the bank readiness signals using a state machine coupled to the memory bus is taught as the MCT 200 handles generation, prioritization and management of operations with the memory (col.5, lines 26-30).

Regarding claim 12, Novak teaches that wherein generating comprises:

sending a memory transaction to a memory bank; clearing the bank readiness signal for the memory bank at approximately the time of sending the memory

transaction to the memory bank; and setting the bank readiness signal for the memory bank a predetermined period of time after sending the memory transaction to the memory bank (col.9, lines 22-26 and col.11, lines 12-22).

Response to Applicant's Arguments

7. Applicant's arguments filed 02/18/2005 regarding claims 1-6 have been fully considered but they are not persuasive.

In response to the applicants' argument that Novak fails to teach or suggest an arbiter simultaneously coupled to each of the plurality of memory transactions and configuration to generate a plurality of bank readiness signals (see applicant's remarks page 7 and 9, regarding claims 1 and 13), it is noted that this limitation is taught as an arbiter (Fig.2, SPM 370) simultaneously coupled to each of the plurality of memory transactions (it is inherent that the SPM 370 coupled to each of the plurality of memory transaction since the SPM 370 selects an operation to be sent to the memory, in order to select an operation, SPM has to coupled to each memory transactions, in addition, Fig.2 of Novak clearly shows that three queues 340,350 and 360 simultaneously connected to the SPM) and configured to generate a plurality of bank readiness signals (it is taught as the requester send to the arbiter will assert the bank readiness signals). The applicant argued that Fig.2 of Novak shows that only the bottom entry of each queue is connected to the multiplexer, the Examiner doesn't agree with it since Fig.2 of Novak clearly shows that three queues 340,350 and 360 simultaneously connected to the SPM (see double lines and bi-directional arrows between SPM and 340,350,360)

8. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

9. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 571-272-4213. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone numbers for the organization where this application or proceeding is assigned are 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Jasmine Song

Patent Examiner

November 9, 2005

FOR

Mano Padmanabhan

Supervisory Patent Examiner

Technology Center 2100

GARY PORTKA
PRIMARY EXAMINER